Modeling-Based Optimization of a Single-Photon Avalanche Diode: Towards Integrated Quantum Photonics Devices Operating at Room-Temperature

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***Abstract*—Single-photon avalanche diodes (SPADs) are emerging as a cost-effective and practical alternative to superconducting nanowire single-photon detectors (SNSPDs), especially for integrated quantum photonics. While SNSPDs exhibit excellent performance such as fast response time and high detection efficiency, their reliance on a cryogenic cooling system results in high cost and power consumption as well as limited suitability for portable devices. In contrast, SPADs can operate at room temperature, eliminating the need for a bulky cooling system and significantly reducing the overall cost. Compared to SNSPDs, however, further optimization of SPAD performance is highly required. In this paper, the SPAD guard-ring (GR) structure is optimized with accurate SPAD device modeling and TCAD simulation, aiming to enhance their suitability for integrated quantum photonics applications. It is demonstrated that the GR-optimized SPAD can reduce internal series resistance and extend its avalanche multiplication region. As a result, the avalanche multiplication region is expanded by approximately 20% , and the peak photon detection probability at a wavelength of 425 nm is increased by 48% . This improvement is achieved while maintaining a low dark count rate of 3.9 cps/μm^2 at an excess bias voltage of 3 V. Additionally, the reduced series resistance enables an increase in current gain and a faster slew rate, which results in much lower timing jitter.**

***Index Terms*—Detector, device optimization, diode, equivalent circuit model, integrated quantum photonics, modeling, optical sensing, optical sensor, photodetector, quantum applications, quantum key distribution (QKD), single-photon avalanche diode (SPAD), single-photon detector, TCAD simulation.**

I. Introduction

A SINGLE-PHOTON avalanche diode (SPAD) operates under the Geiger mode by applying a reverse bias voltage exceeding its breakdown voltage (V_{BD}). When a photon enters the device, it generates an electron-hole pair, which can trigger avalanche multiplication through impact ionization. Due to its high sensitivity and the unique feature in that each photon results in a single digital pulse output, SPADs have been widely used in various optical distance measurement systems [1], [2], [3], [4], [5], [6], [7]. A key advantage of SPADs is their ability to operate at room temperature [8], [9], and thanks to this, SPADs can overcome the limitations of superconducting nanowire single-photon detectors (SNSPDs) [10], which require a cryogenic cooling system, restricting their applications and leading to significant power consumption [11], [12], [13], [14], [15], [16], [17], [18]. Additionally, CMOS-based SPADs offer notable advantages in terms of cost-effectiveness and compatibility with existing integrated circuits. Leveraging these benefits, recent research on SPAD-based integrated quantum photonics has gained considerable attention [19]. Na et al. [20] demonstrated that SPADs with an optimized structure can facilitate efficient integration with photonic circuits. Moreover, Zeng et al. [21] highlighted the potential of room-temperature SPADs in quantum key distribution systems, emphasizing their advantages in reducing system complexity. However, compared to SNSPDs, SPADs still require further improvements in timing jitter and detection efficiency.

In this paper, an equivalent circuit model for the SPAD is implemented through S-parameter measurement. With a ground-signal-ground (GSG) pad [22], [23], we can calibrate out the errors and losses in the measurement system and also remove the parasitic components of the device under test (DUT). Modeling results show that the conventional P+ and N-well (NW) junction SPADs with a high-voltage P-well (HVPW) guard ring (GR), increase internal series resistance mainly by elongating the current path, reducing current gain and consequently requiring higher resistance for quenching. This negatively affects the

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dead time and timing jitter of the device. GR optimization is performed to reduce the high series resistance induced by the HVPW-GR and also expand the avalanche multiplication region into the GR area, thereby achieving a higher photon detection probability (PDP). To achieve this, the HVPW-GR is replaced by a virtual GR that leverages the retrograded doping of the deep NW (DNW) while maintaining the GR spacing. This enables the p-type epitaxial (P-EPI) layer to function as a GR without requiring a separate physical layer. The model's parameters of the GR-optimized SPAD are compared with those of the HVPW-GR SPAD, demonstrating a reduction in series resistance. Furthermore, the junction capacitance increases, confirming the expansion of the avalanche multiplication region to meet optimization goals. TCAD simulation using Sentaurus TCAD is employed for parameter extraction and comparison of electric-field (E-field) profiles, with performance improvements validated by measuring SPAD characteristics such as current-voltage (I-V) characteristics, light emission test (LET), dark count rate (DCR), PDP, and timing jitter. As a result, the avalanche multiplication region shows about 20% expansion, as identified in the LET results, modeling analysis, and E-field profiles obtained from TCAD simulation. This enlargement leads to an improved fill factor, increasing from 51% to 73% , and a remarkable enhancement in PDP at 425 nm, rising from 34.13% to 50.63% —a 48% improvement compared to the HVPW-GR SPAD. DCR levels, including afterpulses, remain low, 3.9 cps/μm^2 at the same excess bias voltage (V_{EX}) of 3 V in the GR-optimized SPAD. Timing jitter is measured at a wavelength of 510 nm, near the device's peak PDP, under V_{EX} of 3 V, and the full width at half maximum (FWHM) of the timing jitter is dramatically improved by about 3.9 times from 224 to 57 ps.

This paper proceeds as follows: Section II discusses the SPAD modeling work conducted to optimize the GR structure. Additionally, a comparison of E-field profiles between the HVPW-GR SPAD and the GR-optimized SPAD using TCAD simulations is provided. Section III presents the experimental results that validate the modeling analysis. Finally, Section IV concludes the study.

II. Device Structure and Modeling Analysis

A. Device Structure and Its Equivalent Circuit Model

When a reverse bias voltage exceeding V_{BD} is applied to a SPAD, a photon-generated carrier can trigger an avalanche multiplication through impact ionization. Avalanche multiplication creates a substantial amount of electron-hole pairs. Assuming that generated carriers travel at saturation velocity, they induce changes in the E-field, resulting in voltage variations. The relationship between the voltage change caused by the carriers in the avalanche multiplication region and the space-charge limited current due to carrier motion with saturation velocity allows for modeling a space-charge resistance, R_{SPAD} [24]. R_{SPAD} is the resistance along the path of avalanche current, directly related to current gain, and is a key parameter that defines avalanche multiplication. Additionally, the series resistance in SPADs can lead to voltage drops, further decreasing current gain, and the junction capacitance is proportional to the multiplication region so that it can represent the area of the multiplication region. An equivalent circuit model can be built with these device parameters, enabling a deep analysis of SPAD characteristics.

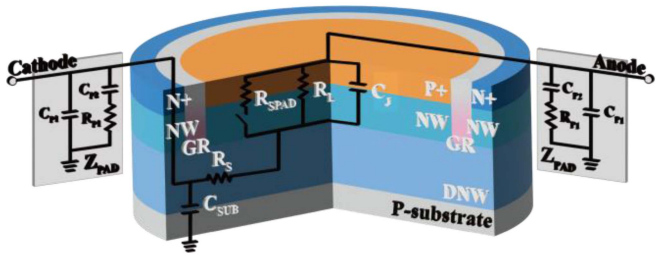

Fig. 1. Device structure and equivalent circuit model of the HWPW-GR SPAD.

To eliminate the parasitic effects of the pads and isolate the SPAD's intrinsic properties, a GSG pad was designed. The impedance characteristics of the SPAD, including the GSG pad, were extracted from S-parameter measurements. The pad's S-parameters were measured separately to remove the pad's influence. For accurate analysis of capacitance and other components, measurements were made up to 20 GHz using a vector network analyzer (VNA).

Fig. 1 shows the model of a P+/N-well junction SPAD with HVPW-GR, fabricated in a 55 nm bipolar-CMOS-DMOS (BCD) technology. The active area was designed with a diameter of 13.5 μm, while the GR size was set to 1.8 μm. In this model, R_S represents the series resistance, C_J is the junction capacitance, and R_{SPAD} is the space-charge resistance. R_L represents the leakage resistance in the depletion region, which is large enough to make leakage negligible in SPAD. C_{SUB} denotes the parasitic capacitance between the deep N-well and the substrate, while C_{P1}, C_{P2}, and R_{P1} model the parasitic components due to the pad's bottom metal layer and leakage between the pad and substrate. R_{P1} includes the parasitic components from the slit in the shield metal.

B. Parameter Extraction

The parameter values for each model were first calculated using known equations and then fine-tuned through the Advanced Design System (ADS). The values of C_J and R_{SPAD} were calculated using the following equations [24]:

$$C_J = \frac{\varepsilon_s A}{W_D},\ R_{SPAD} = \frac{(W_D - \chi_A)^2}{2A\varepsilon_s \nu_s} \tag{1}$$

W_D is the width of the depletion region, A is the cross-sectional area of the junction, χ_A is the avalanche width, ε_s is the material permittivity, and ν_s is the carrier saturation velocity. The values for W_D and χ_A were obtained through TCAD simulations.

Previous modeling works on avalanche photodiodes (APDs) have reported that the values of C_J and R_S do not change significantly beyond the breakdown voltage V_{BD} under different bias conditions [25]. R_{SPAD}, on the other hand, represents the resistance associated with avalanche multiplication occurring

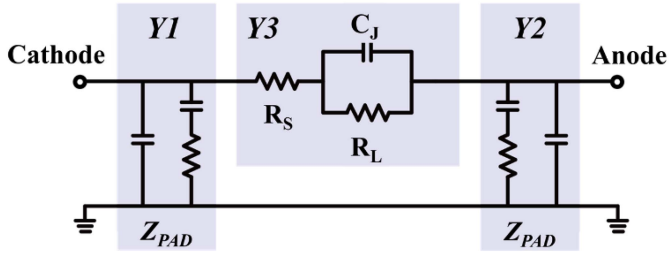

Fig. 2. Equivalent circuit model with π network assumption at V_{BD}.

TABLE I
COMPARISON OF EXTRACTED DEVICE PARAMETERS OF HVPW-GR SPAD AND P-EPI-GR SPAD AT $V_{EX} = 3$ V

Z_{PAD}		HVPW-GR SPAD		P-EPI-GR SPAD	
C_{P1}	45 fF	R_{SPAD}	130 Ω	R_{SPAD}	108 Ω
C_{P2}	225 fF	R_S	1.9 kΩ	R_S	350 Ω
R_{P1}	110 Ω	C_J	28 fF	C_J	33.6 fF
		C_{SUB}	6 fF	C_{SUB}	6 fF

under V_{BD}+V_{EX} conditions. Therefore, the parameter extraction was first carried out at V_{BD}, excluding R_{SPAD}, followed by the extraction of R_{SPAD} at V_{EX} of 3 V by fitting the measurement data without any other parameter changes.

Assuming a π network model for the SPAD equivalent circuit at $V_{BD,}$ as shown in Fig. 2, the *Y3* part can be calculated as $-Y_{12}$. Using the following equations, R_S corresponds to the real part of Y_{12}, and C_J is dominated by the imaginary part of Y_{12}, allowing for fine-tuning.

$$j\omega C_J + \frac{1}{R_L} \approx j\omega C_J,\ Y_{12} \approx j\omega C_J \parallel \frac{1}{R_S} \tag{2}$$

$$Y_{12} \approx \frac{j\omega R_S C_J}{R_S + j\omega C_J} = \frac{\omega^2 R_S {C_J}^2 + j\omega {R_S}^2 C_J}{{R_S}^2 + \omega^2 {C_J}^2} \tag{3}$$

$$\therefore Y_{12} \approx \frac{\omega^2 {C_J}^2}{R_S} + j\omega C_J \ \left(\because {R_S}^2 \gg \omega^2 {C_J}^2\right) \tag{4}$$

C. Modeling Results

The HVPW-GR SPAD modeling results shown in Table I reveal that, as the current path increases, the series resistance also increases. When the series resistance increases, the current gain decreases, requiring a larger quenching resistance, which increases dead time. For faster photon detection, it is advantageous to use a smaller quenching resistance. GR optimization was conducted to reduce the series resistance. The use of the P-EPI-GR as shown in Fig. 3 not only reduces the current path but also extends the multiplication region as it is not blocked by the physical GR. This was aimed at increasing the PDP for high detection efficiency. The region labeled as the 'simulation region' in Fig. 3 was simulated using TCAD in Figs. 5 and 6 to verify this. The designed SPAD with the P-EPI-GR was also modeled to extract device parameters. In Fig. 4, the simulated S_{22} and output impedance characteristics of the HVPW-GR

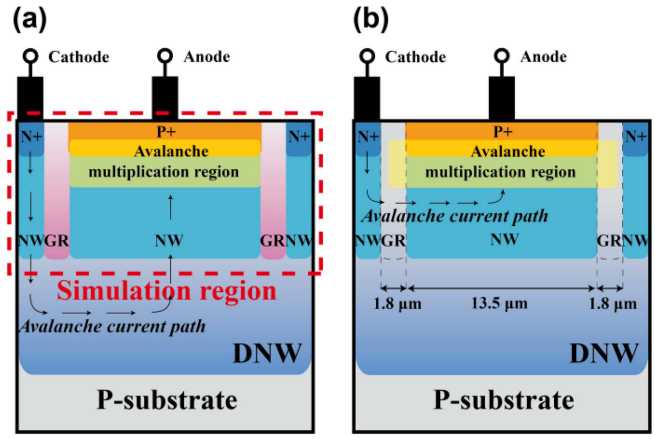

Fig. 3. Device structure of the (a) HVPW-GR SPAD and (b) GR-optimized SPAD.

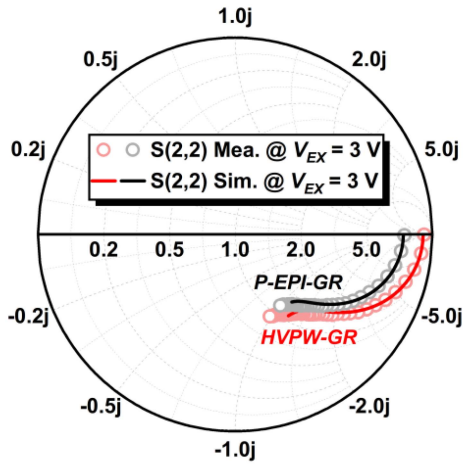

Fig. 4. Measured vs. simulated output impedance characteristics at $V_{EX} = 3$ V for the HVPW-GR SPAD and P-EPI-GR SPAD.

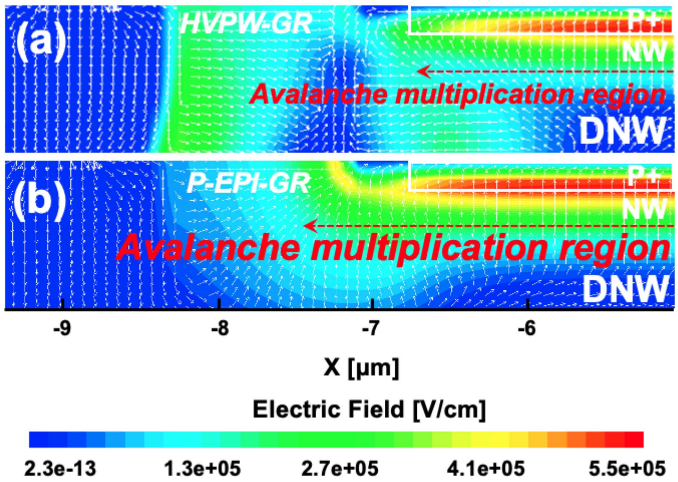

Fig. 5. TCAD simulation results at $V_{EX} = 3$ V: electric-field distribution of the (a) HVPW-GR SPAD and (b) P-EPI-GR SPAD.

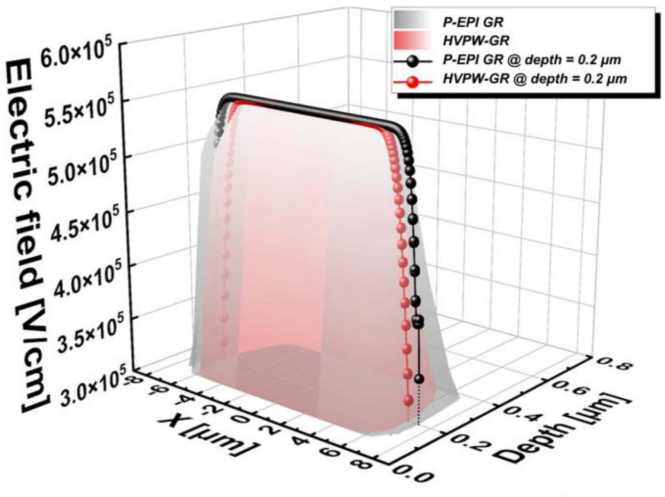

Fig. 6. 3D electric-field profiles above the critical electric field of 3×10^5 V/cm for the HVPW-GR SPAD and P-EPI-GR SPAD at $V_{EX} = 3$ V.

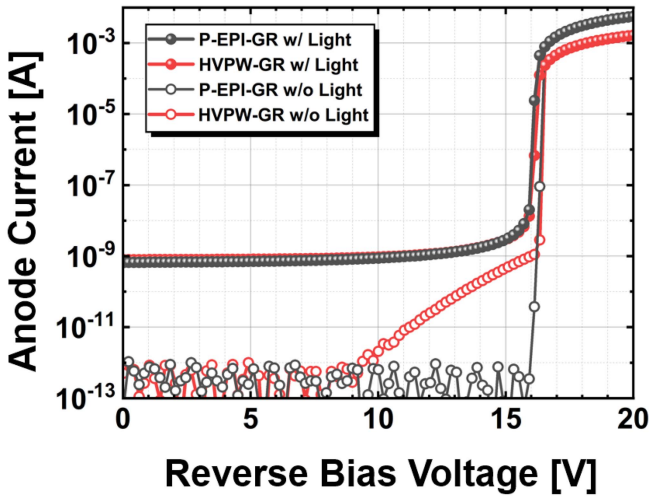

Fig. 7. I-V characteristics comparison between the HVPW-GR SPAD and P-EPI-GR SPAD at room temperature.

SPAD and P-EPI-GR SPAD, based on their equivalent circuit models, are compared with the measured S_{22}. The results show a strong agreement between the simulation and measured data, demonstrating the accuracy of the modeling. The device parameters' values are compared in Table I.

From the device parameter values, it is found that in the GR-optimized SPAD, R_S decreased by approximately 5.4 times, R_{SPAD} decreased by 1.2 times, and C_J increased by 1.2 times. Due to the lowered resistance in the P-EPI-GR SPAD, the impedance characteristics appear closer to the origin on the Smith chart, indicating a reduced impedance as shown in Fig. 4. According to (1), R_{SPAD} is inversely proportional to the cross-sectional area of the active area, A, while C_J is directly proportional to it. Thus, the 1.2 times difference in R_{SPAD} and C_J compared to the conventional HVPW-GR SPAD indicates that the avalanche multiplication region expanded by 1.2 times into the designed GR area. Furthermore, the 5.4 times reduction in R_S signifies a significantly shortened current path, suggesting that the current gain may have increased to a similar extent. Modeling results show that the original optimization design goals are successfully achieved.

D. TCAD Simulation Analysis

TCAD simulations were employed to extract SPAD model parameters and compare the E-field profiles of the conventional HVPW-GR SPAD and the optimized P-EPI-GR SPAD. Fig. 5 provides a magnified view of the E-field profile in the part of junction and GR region in the SPADs. In the P-EPI-GR structure, the avalanche multiplication region extends into the GR area since no physical layer obstructs the junction, as shown in Fig. 5(b). This expansion aligns with the trends observed in the modeling results. Additionally, the simulation shows that premature edge breakdown (PEB) is effectively prevented in both SPADs.

As a higher reverse bias voltage is applied to the SPAD, the E-field across the depletion region strengthens, causing externally injected carriers to move with greater force. When the applied voltage reaches a sufficient level, the E-field strength becomes large enough to reach a threshold of 3×10^5 V/cm, known as the critical E-field, where carriers collide, triggering avalanche multiplication via impact ionization. Fig. 6 shows the TCAD simulation results depicting the 3D profile of regions where the E-field exceeds the critical E-field threshold. This corresponds to the avalanche multiplication region, which has an approximate thickness of 0.3 μm. In the HVPW-GR SPAD, the E-field profile in the GR region does not exceed the critical E-field, as shown in Figs. 5 and 6. The carrier movement in Fig. 5 indicates that the junction is completely blocked. Additionally, a shorter carrier movement path is observed in the P-EPI-GR SPAD. The E-field distribution comparison and carrier movement in the TCAD simulation results align with the modeling results, specifically showing a reduction in R_{SPAD} and R_S, along with an increase in C_J.

III. Experimental Results

A. Current-Voltage (I-V) Characteristics

The I-V characteristics were measured by accumulating the output current from the SPAD's anode at each reverse bias voltage over a fixed period under dark and low light conditions. The current flowing in the absence of light is referred to as the dark current, while the current measured under illumination is defined as the sum of dark current and photocurrent. Ideally, when avalanche multiplication occurs, the current would rise infinitely. However, due to space-charge resistance, R_{SPAD}, the current saturates at a certain level [24]. Using these I-V characteristics, we compared the V_{BD} and current gain of a conventional HVPW-GR SPAD with a GR-optimized SPAD. Both SPADs have the same P+/N-well junction, resulting in the same V_{BD} of approximately 16 V and identical dark current characteristics up to a reverse bias voltage of about 7 V, as shown in Fig. 7. In the case of the HVPW-GR SPAD, defects induced by

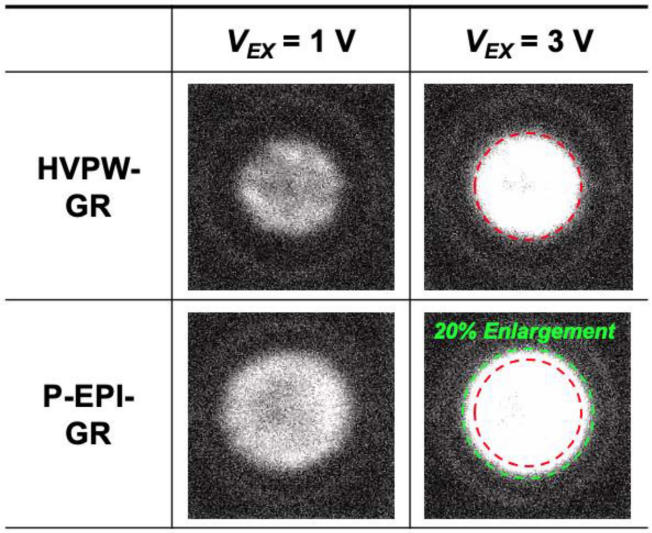

Fig. 8. LET results at room temperature under $V_{EX} = 1$ V and 3 V for the HVPW-GR SPAD and P-EPI-GR SPAD.

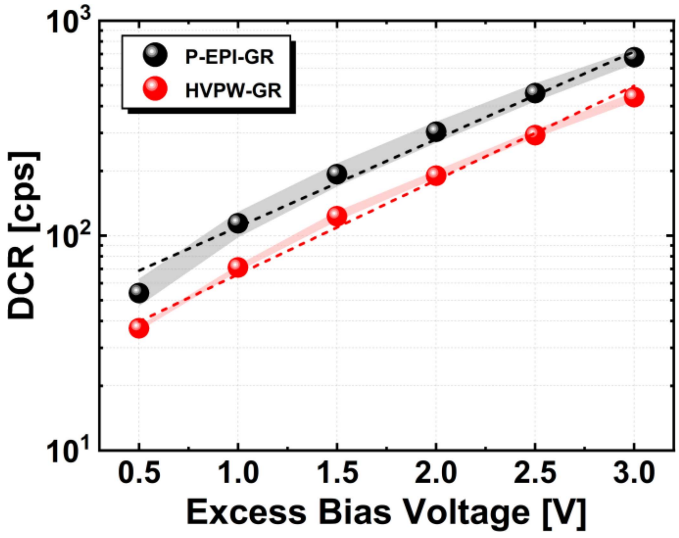

Fig. 9. DCR comparison between the HVPW-GR SPAD and P-EPI-GR SPAD at V_{EX} ranging from 0.5 to 3 V at room temperature.

the high-energy implantation process make it more susceptible to lateral leakage, leading to an increase in dark current beyond this voltage. In contrast, the optimized P-EPI-GR SPAD exhibits a reduced dark current since it eliminates the need for a separate GR formation process. However, this lateral leakage does not contribute to the DCR as it does not flow through the avalanche junction.

While R_{SPAD} predominantly affects the saturation current gain as it is the path of avalanche current, series resistance contributes to the voltage drop, thereby affecting the gain as well. As demonstrated in the modeling results in Section II, the P-EPI-GR SPAD exhibits higher current gain due to its lower series resistance, which results from a shorter current path and a reduced R_{SPAD} caused by the expanded multiplication region.

B. Light Emission Test (LET)

LET allows for the observation of the light emission area in real time. The SPAD device is placed inside a dark box, and probes are positioned on the cathode and anode pads to apply a reversed bias voltage. When the applied voltage exceeds the V_{BD}, avalanche multiplication occurs, generating electron-hole pairs (EHPs). As some of the EHPs are recombined, light is emitted in the visible or near-infrared wavelength range. This emitted light is detected using a high-sensitivity image sensor or camera. To compare the avalanche multiplication regions of the two SPADs by examining the width of the light emitting areas, LETs were conducted at V_{EX} of 1 V and 3 V, confirming that a stronger E-field formed as V_{EX} increased to 3 V, leading to uniform avalanche activity across the active area. As shown in Fig. 8, despite P-EPI-GR not being as physical as HVPW-GR, well-optimized P-EPI-GR effectively prevented PEB, as no light emission was observed near the edges.

Additionally, using the P-EPI-GR allowed carriers generated by avalanche multiplication to extend into the GR area, resulting in a light-emitting area approximately 1.2 times larger than the HVPW-GR SPAD. This matches well with the modeling results, which showed 1.2 times increase in C_J, indicating a wider avalanche multiplication region.

C. Dark Count Rate (DCR)

DCR represents the false output signal generated without light as if a photon had been detected. DCR can arise from various sources, primarily from carriers generated in the avalanche junction due to thermal noise, band-to-band tunneling, or trap-assisted tunneling (TAT). A high DCR can make the distinction between actual photon events and noises difficult.

It also impacts PDP measurements and increases power consumption. The DCR for both the HVPW-GR and P-EPI-GR SPAD was characterized by measuring under room temperature conditions, with V_{EX} ranging from 0.5 V to 3 V in 0.5 V increments. Considering die variation, DCR measurements were conducted on five different dies per device, and the average values were plotted as markers in Fig. 9. Although the P-EPI-GR SPAD showed a slight increase in DCR due to its proportional relationship with the active area's cross-sectional size, and increased current gain, it remained low at 3.9 cps/μm^2. The P-EPI-GR SPAD exhibits slightly higher DCR than the proportional rate due to the multiplication region extending deeper into the GR area, but the difference is not significant. The dashed trend lines in Fig. 9 demonstrate that both devices exhibit a similar trend of increasing DCR with higher excess bias voltage, as their device structures are identical except for the GR structure.

Afterpulses, another noise component in SPADs, occur when photon-generated carriers are trapped within the device's defect and released after a short period, causing a false avalanche event. Since afterpulses occur shortly after a previous avalanche event, afterpulsing probability is determined by histogramming the time intervals between avalanche events. Events occurring at longer time intervals are unlikely to be afterpulses. This longer period, such as 15–20 μs, is used as a reference, and

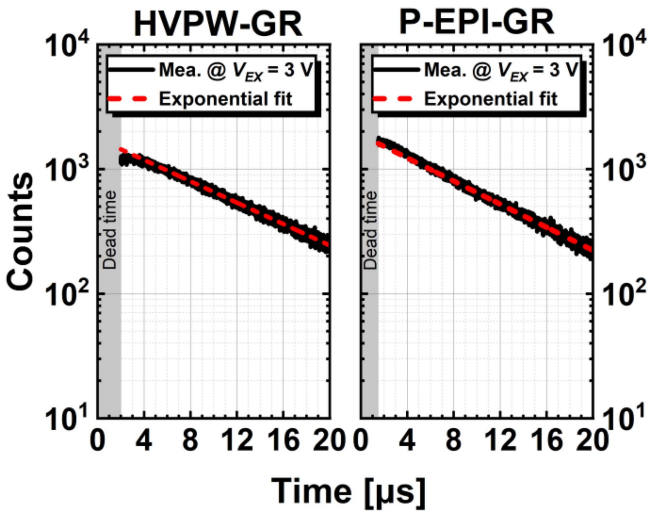

Fig. 10. Measured inter-avalanche events of the HVPW-GR SPAD and P-EPI-GR SPAD at $V_{EX} = 3$ V at room temperature.

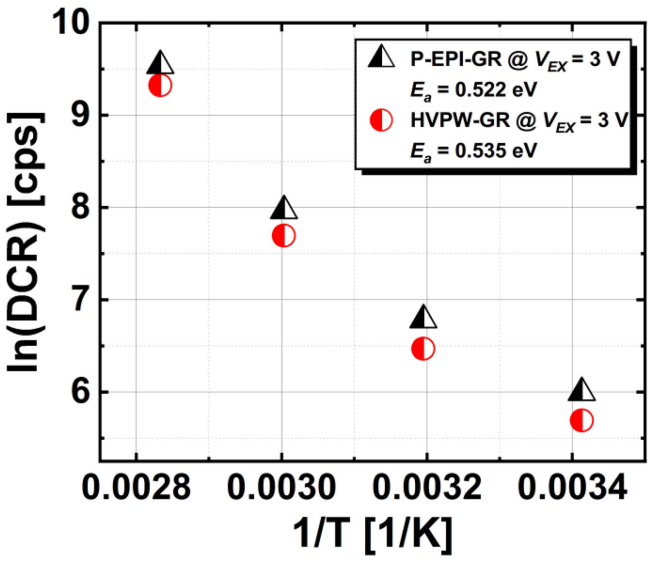

Fig. 11. The Arrhenius plot of the HVPW-GR SPAD and P-EPI-GR SPAD, measured at $V_{EX} = 3$ V.

an exponential curve is fitted to the distribution. Any counts exceeding this exponential fit in the short time period are considered afterpulses, and the ratio of these counts to the total count is defined as the afterpulsing probability. In Fig. 10, the afterpulsing probability was measured at V_{EX} of 3 V in room temperature conditions, with a dead time of 2 μs for the HVPW-GR SPAD and 1.5 μs for the P-EPI-GR SPAD. The results confirmed that both the HVPW-GR SPAD and P-EPI-GR SPAD exhibit no significant afterpulsing up to their respective dead times.

Fig. 11 illustrates the trend of DCR variation with temperature for both SPADs. Measurements were conducted at a V_{EX} of 3 V, ranging from 20 °C to 80 °C in 20 °C intervals, and an Arrhenius plot was used to extract the activation energy (E_a). As with the

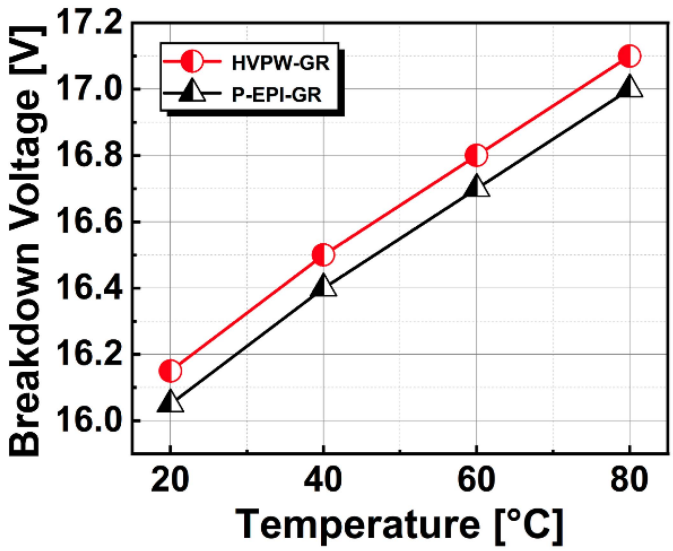

Fig. 12. Measured V_{BD} variation with temperature of the HVPW-GR SPAD and P-EPI-GR SPAD.

DCR measurements at room temperature, as shown in Fig. 9, the P-EPI-GR SPAD exhibited a slightly higher DCR, but the difference between the two devices was minimal. Moreover, the DCR variation trend with temperature was nearly identical for both SPADs. The activation energy values were 0.535 eV for the HVPW-GR SPAD and 0.522 eV for the GR-optimized SPAD, suggesting that the dominant DCR sources are the same—likely stemming from TAT processes.

Fig. 12 depicts the variation in V_{BD} with temperature for both SPADs, measured across a range of 20°C to 80°C. The HVPW-GR SPAD consistently exhibited a V_{BD} approximately 0.1 V higher than the P-EPI-GR SPAD throughout the temperature range. However, this difference is within the margin of die variation and can be considered negligible. Both SPADs showed the same trend in V_{BD} variation with temperature, with a temperature coefficient of 15 mV/K. This indicates that both devices operate stably at room temperature and are minimally affected by temperature changes, ensuring reliability even when integrated into portable applications for outdoor environments in integrated quantum photonics.

D. Photon Detection Probability (PDP)

PDP is one of the most critical characteristics determining the performance of a system when SPADs are used as detectors in various applications, including the quantum applications mentioned above. Due to the inherent properties of Si-based SPADs, they exhibit high PDP in the visible spectrum. Figs. 13 and 14 show the PDP results measured at room temperature for both the HVPW-GR SPAD and P-EPI-GR SPAD, with V_{EX} ranging from 1 V to 3 V in 1 V increments and wavelengths from 400 nm to 950 nm in 25 nm intervals. Both SPADs exhibit the highest PDP peak at 425 nm in the green light spectrum. This peak is attributed to the significant doping concentration difference in the P+/N-well junction, which creates a strong E-field in a

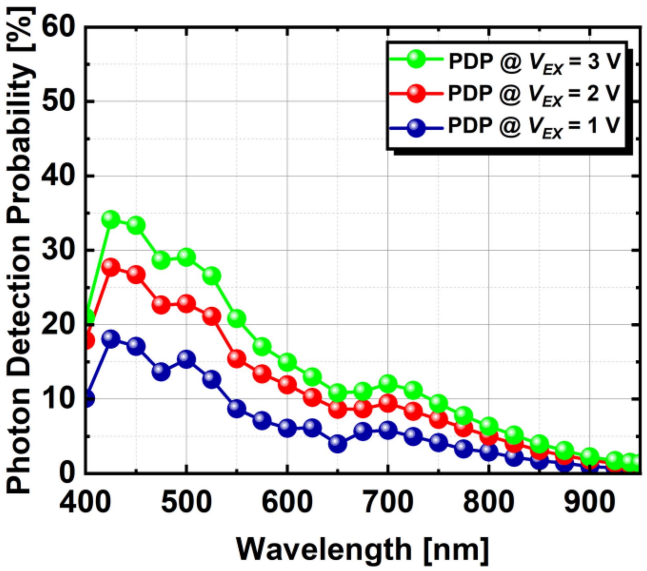

Fig. 13. PDP of the HVPW-GR SPAD at room temperature.

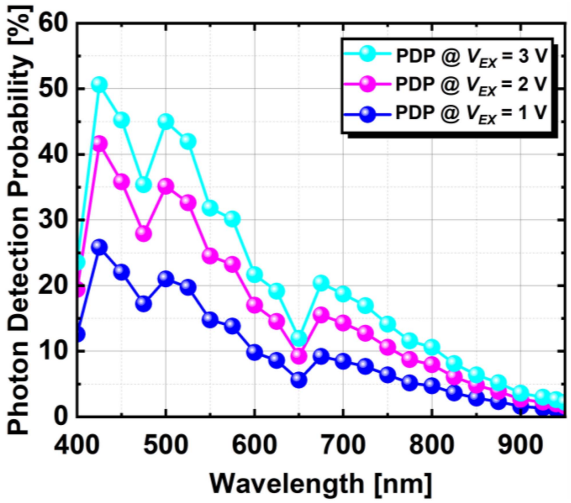

Fig. 14. PDP of the P-EPI-GR SPAD at room temperature.

thin layer. Consequently, many photon-generated carriers produced by shorter wavelengths can easily reach the avalanche multiplication region. In Fig. 13, the HVPW-GR SPAD shows a PDP peak of 34.13% at a V_{EX} of 3 V at 425 nm. The optimized P-EPI-GR SPAD demonstrates a peak of 50.63% at the same wavelength and voltage, representing an improvement of approximately 48% over the conventional HVPW-GR SPAD, as shown in Fig. 14. This improvement is due to the extension of the avalanche multiplication region, as well as the expanded carrier collection region at the periphery, which allows for the absorption of more carriers. Both SPADs have a similar trend of relatively lower PDP at higher wavelengths due to the shallow formation of the junction with a strong E-field.

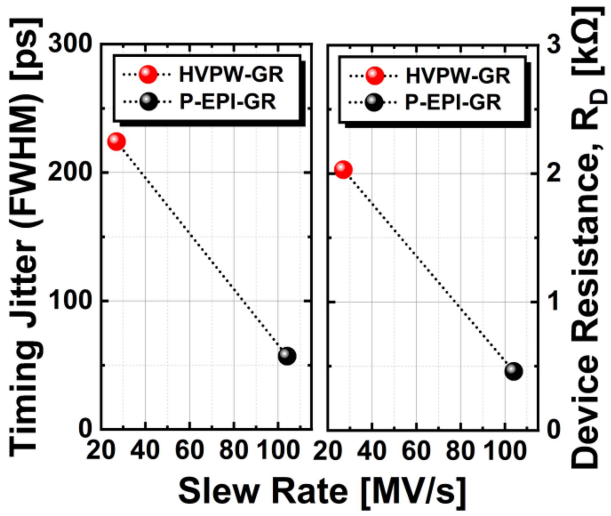

Fig. 15. Measured slew rate vs. timing jitter at 510 nm wavelength and device resistance of the HVPW-GR SPAD and P-EPI-GR SPAD at $V_{EX} = 3$ V at room temperature.

E. Timing Jitter

Along with PDP, timing jitter is one of the critical characteristics for achieving fast response speed in integrated quantum photonics. Timing jitter was measured at a wavelength of 510 nm, close to the peak PDP, under room temperature and a bias condition of V_{EX} of 3 V. According to [26], the root-mean-square (RMS) timing jitter is inversely proportional to the slew rate measured at 50% of the pulse's amplitude. A slower slew rate makes the signal more susceptible to distortion from small time variations, increasing the timing jitter. Since RMS timing jitter assumes a Gaussian distribution of the measurement results, it can be expressed as the standard deviation, equivalent to the FWHM divided by a factor of $2\sqrt{2ln2}$. In [27], the SPAD's quenching time constant is determined by the following equation.

$$\therefore \tau_q \approx (C_D + C_L) \times R_D \tag{5}$$

Based on the modeling results, the device resistance R_D can be simplified to $R_S + R_{SPAD}$, while the device capacitance C_D adds to the load capacitance C_L. Consequently, R_D predominantly affects the quenching time constant. Since this is directly related to the slew rate, a larger R_D results in a slower slew rate, increasing timing jitter and leading to slower response characteristics.

Fig. 15 illustrates the relationship between device resistance extracted from modeling results, timing jitter, and slew rate measurements. The GR optimization in the P-EPI-GR SPAD significantly reduced R_D, and a similar proportional improvement in timing jitter was observed. The slew rate increased from 27 MV/s to 104 MV/s, approximately a 3.85-fold improvement, while the timing jitter based on FWHM decreased from 224 to 57 ps, showing a 3.92-fold reduction. This inverse relationship between slew rate and timing jitter is clearly demonstrated.

IV. Conclusion

In this study, the SPAD is optimized for integrated quantum photonics, targeting enhanced detection efficiency and fast response characteristics. The optimization focused on the GR structure, aiming to reduce series resistance, R_S and enlarge the multiplication region, based on an equivalent circuit model that accurately reflects the SPAD's impedance characteristics. TCAD simulations are employed to extract device parameters for the model and to compare the E-field profiles. Experimental results are consistent with the modeling results. Specifically, the reduction in R_S in the optimized P-EPI-GR SPAD model demonstrates the decrease of internal series resistance, leading to an increased current gain and faster slew rate, which contributed to reduced timing jitter. The increased C_J is also associated with the expanded emission region of LET, leading to improved PDP. However, this also causes a slight increase in DCR, which remains at an acceptably low level. These results confirm the success of the modeling-based optimization, demonstrating that the approach is effective. The proposed modeling framework holds the potential for continuous optimization tailored to future target applications.

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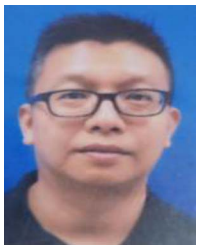

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